VERIFICATION OF TRANSLATION

I, "Satoshi Hoshikoshi", a translator with an employee of "Fukumori Patent Office" (Address: 2F FUJI BLDG., 5-11, Kudan-Minami 4-chome, Chiyoda-ku, Tokyo 102-0074, Japan), hereby declare as follows:

That I am familiar with the Japanese and English languages;

That I am capable of translating from Japanese to English;

That the corrected translation attached hereto is a true and accurate translation of Japanese language Application titled, "RFID タグ装置" and having Japanese Application No. 2004-054933, filed on February 27, 2004;

That all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true;

And further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any registration resulting therefrom.

By Sat. Hos

Executed this 20th day of October, 2011

Witness Hitoshi Takahashi

CLAIMS

1. An RFID tag device comprising a divided microstrip antenna, and a power receiving circuit based on a combination of a stub resonance-based, impedance transformation RF boosting scheme and a ladder boosting/rectifying scheme, and a passive QPSK modulation scheme is usable as a modulation method, wherein a dividing position of the divided microstrip antenna is slightly deviated from a longitudinal center point across strip conductors.

2. The RFID tag device according to claim 1, wherein impedance modulation elements of the divided microstrip antenna are respectively connected to opposite ends in a strip conductor width direction so as to connect divided conductors.

3. The RFID tag device according to claim 2, wherein the impedance modulation elements constitute a voltage or current controlled three-terminal element using a transistor, rather than a diode.

4. The RFID tag device according to any one of claims 1 to 3, wherein an extremely small capacitance of 1 pF/GHz or less is used for connecting the power receiving circuit and an antenna feeding point to perform high-impedance capacitive feeding.

5. The RFID tag device according to any one of claims 1 to 4, wherein capacitive load impedances in a stub resonator and a ladder boost rectifier circuit of the power receiving circuit are parallel resonant, and further, the capacitive feeding impedance are series resonant.

6. The RFID tag device according to any one of claims 1 to 5, wherein when considering longitudinal connections of capacitors in the ladder boost rectifier circuit of the power receiving circuit as GND- and receiving-side rails, capacitor capacitance of the receiving-side rail is smaller than that of the GND-side rail, a first diode between GND and a receiving point is eliminated, and a high-frequency and high-impedance input is receivable by a DC short.

7. The RFID tag device according to any one of claims 1 to 6, wherein a logic circuit including a 1/4 frequency divider, a shift register and a data selector is used in the passive QPSK modulation method.

8. The RFID tag device according to claim 7, wherein MPSK modulation is

applied by using a 1/M frequency divider, an M-stage shift register and an M-input data selector.

9. The RFID tag device according to any one of claims 1 to 7, wherein information is recorded to a memory in units of two bits in accordance with the passive QPSK modulation method.

10. The RFID tag device according to any one of claims 1 to 7 and claim 9, including an output timing generator circuit for obtaining an output enable signal in the passive QPSK modulation method.

11. The RFID tag device according to claim 10, wherein the output timing generator circuit generates a train of pulses with a random delay time having a fixed width and a fixed frame cycle, based on a source voltage size and a clock signal.

DESCRIPTION

TITLE OF THE INVENTION: RFID Tag Device

TECHNICAL FIELD

[0001] The present invention relates to RFID tag devices, and specifically to an RFID tag device based on passive modulation, but capable of performing QPSK modulation for wireless communication by using a loop antenna or a dipole antenna.

BACKGROUND ART

[0002] Patent Document 1: Japanese Laid-Open Patent Publication No. 10-2242626 (Tags for radio frequency identification communication systems) RFID is wireless equipment for identifying mobile objects, which is attached to or held by a commodity, a person, a car, a road sign, etc., and in response to a radio wave from an interrogator (a reader/writer), notifies individual information and position information to the interrogator.

[0003] The RFID is considered not only as an alternative to the barcode, but also as elemental technology for implementing an entirely new infrastructure for a future network community. The research and development of RFID currently underway mainly concentrates on communication within a relatively short range of several tens of centimeters, but if it is possible to realize low-cost small RFID tags capable of communication from relatively afar, such as from about 10 meters away, the application range will be conceivably further extended.

[0004] When such is attached to a commodity, a person, a car or a road sign, for example, its individual information and position information are read by a mobile object from 10 m away, making it possible to readily enjoy safety and convenience.

[0005] The above Patent Document 1 describes a conventional passive RFID tag device. According to this, the conventional passive RFID tag device is basically configured as shown in FIG. 1, and therefore has a problem that its possible communication range is short for the following reasons.

(1) A response signal is created by regularly changing impedance Zv between an antenna feeding point and GND to repeat reflection and absorption of incident radio waves, so that the transmission output (conversion efficiency) is low, and the load impedance Zv is applied between the feeding point and GND, resulting in considerable loss of received power.

(2) The source voltage for a control circuit is created by directly diode-rectifying an RF signal received at the antenna feeding point, and therefore the output voltage is low.

(3) ASK or BPSK is used as a subcarrier modulation scheme, and therefore the amount of information that can be transmitted per transmission power is small.

DISCLOSURE OF THE INVENTION

PROBLEM TO BE SOLVED BY THE INVENTION

[0006] The present invention aims to overcome the drawback with the above conventional technology by the configuration shown in FIG. 2, and expand the communication range to several times or more that in the conventional scheme.

MEANS FOR SOLVING PROBLEM

[0007] The main points of the present invention for solving the above problems are as shown below.

[0008] The conventional scheme is based on equilibrium feeding/equilibrium modulation (a two-terminal circuit for antenna operation), whereas a method of the present invention is based on disequilibrium feeding/equilibrium modulation (a three-terminal circuit for antenna operation). The conventional scheme is based on simple rectification of received RF signals, whereas the present invention employs a circuit based on a combination of a stub resonance-based, impedance transformation boosting scheme and a ladder boosting scheme. The conventional scheme is

based on ASK or BPSK modulation, whereas the present invention is based on passive modulation, but can employ a QPSK modulation circuit.

[0009] Specifically, an RFID tag device of the present invention includes a divided microstrip antenna, and a power receiving circuit based on a combination of a stub resonance-based, impedance transformation RF boosting scheme and a ladder boosting/rectifying scheme. A passive QPSK modulation scheme is usable as a modulation method. And a dividing position of the divided microstrip antenna is slightly deviated from a longitudinal center point across strip conductors.

[0010] Also, according to the RFID tag device of the present invention, it is preferred that impedance modulation elements of the divided microstrip antenna are respectively connected to opposite ends in a strip conductor width direction so as to connect divided conductors. A voltage or current controlled three-terminal element using a transistor, rather than a diode, is preferable.

[0011] Further, according to the RFID tag device of the present invention, an extremely small capacitance (1 pF/GHz or less) is preferably used for connecting the power receiving circuit and an antenna feeding point to perform high-impedance capacitive feeding.

[0012] Also, according to the RFID tag device of the present invention, it is preferred that capacitive load impedances in a stub resonator and a ladder boost rectifier circuit of the power receiving circuit are parallel resonant, and further, the capacitive feeding impedance are series resonant.

[0013] Further, according to the RFID tag device of the present invention, it is preferred that when considering longitudinal connections of capacitors in the ladder boost rectifier circuit of the power receiving circuit as GND- and receiving-side rails, capacitor capacitance of the receiving-side rail is smaller than that of the GND-side rail, a first diode between GND and a receiving point is eliminated, and a high-frequency and high-impedance input is receivable by a DC short.

[0014] Also, according to the RFID tag device of the present invention, a logic circuit including a 1/4 frequency divider, a shift register and a data selector is preferably used in the passive QPSK modulation method, and MPSK modulation is preferably applied by using a 1/M frequency divider, an M-stage shift register and an M-input data selector.

[0015] Further, according to the RFID tag device of the present invention,

information is preferably recorded to a memory in units of two bits in accordance with the passive QPSK modulation method.

[0016] Also, the RFID tag device of the present invention preferably includes an timing generator circuit for obtaining an output enable signal in the passive QPSK modulation method, and the output timing generator circuit preferably generates a train of pulses with a random delay time having a fixed width and a fixed frame cycle, based on a source voltage size and a clock signal.

EFFECT OF THE INVENTION

[0017] By employing these configurations, it is made possible to achieve considerable effects as below.

[0018] Disequilibrium feeding and equilibrium modulation (a three-terminal circuit for antenna operation) are employed, and therefore it is possible to achieve the effect of maximizing the reception efficiency of an antenna.

[0019] Also, by employing a circuit based on a combination of a stub resonance-based, impedance transformation boosting scheme and a ladder boosting scheme, it is possible to obtain a reception voltage of five times or more that of conventional schemes.

[0020] Further, by employing a QPSK modulation circuit, but based on passive modulation, it is made possible to transmit information in an amount twice that of the conventional method per unit of transmitting power.

BEST MODES FOR CARRYING OUT THE INVENTION

[0021] An embodiment of the present invention will now be described.

(Example 1)

[0022] FIG. 3 illustrates the basic configuration of an RFID tag device of the present invention. In this figure, the antenna of the RFID tag device includes a ground plane conductor, an insulating layer and a divided strip conductor. The RFID tag device shown in this figure is for use in the 2.45 GHz band, and all specified dimensions are in units of mm. Also, the dividing point of the divided strip conductor is deviated slightly more than equal division in the longitudinal direction, and this feature achieves the effect of maximizing the reception efficiency of the antenna.

[0023] FIG. 4 illustrates the details of the control circuit chip shown in FIG. 3 and connections between the divided strip conductor and the control circuit.

[0024] In FIG. 4, the control circuit chip and the antenna are connected at six points A, B, C, D, E and F. PIN diodes D7 and D8 for impedance modulation are connected between A and B and between D and E, respectively, and a feeding point of the antenna lies between C and F. Here, the point C is slightly deviated from the center point of the strip conductor width, and this feature achieves the effect of maximizing the reception efficiency of the antenna. Also, the point F is connected to the ground plane conductor via a through-hole.

[0025] The operation principle of the power supply circuit in FIG. 4 is shown in FIG. 5. FIG. 5(a) is a boost rectifier circuit called "Cockcroft-Walton circuit", in which a plurality of rectifier diodes and capacitors are connected in a ladder configuration, so that a sine value signal with an amplitude of Vi can be output after being rectified to a DC voltage of K(Vi-lj) greater than Vi [K is the number of ladder steps; lj is a forward drop voltage of a diode]. However, as shown in FIGS. 10 and 11, this circuit has a drawback in that when it is used in a high frequency band (e.g., 2.45 GHz), the junction capacitance of each diode becomes input load and therefore input impedance becomes extremely low, which lowers the output voltage.

[0026] FIG. 5(b) is an operational principle diagram of the boost rectifier circuit of the present invention. An $N\lambda g/4$ short stub (λg is an effective wavelength of the transmission path; N is an odd number being 1 or 3) exhibits an equivalent impedance of an inductance having a high Q-value in a high frequency range with respect to an input signal in the vicinity of λg. Even if a ladder boost section of FIG. 5(b) is a capacitive load, an inductive impedance can be maintained by a parallel resonance operation. On the other hand, in a tank circuit boost section of FIG. 5(b), the inductive impedance and a capacitive feed impedance generate an RF signal, which has a large amplitude of

$$V_L = Vi / (R_L \times wc) >> Vi,$$

between G and F by a series resonance operation, so that the circuit of FIG. 5(b) can obtain a DC output voltage of 20Vi or more.

[0027] FIG. 17 is a behavioral analysis result of the boost rectifier circuit of the present invention, from which it is appreciated how an input voltage of 50 W / -10 dBm (0.07 V) is boosted and rectified to 1 V or more at 2.45 GHz.

[0028] Next, the control circuit chip of FIG. 4 is described in detail.

[0029] When V_{DD} is applied, an oscillator circuit generates a clock signal of

fs. When V_{DD} and the clock signal are applied, an output timing circuit generates a timing signal (an output enable signal) for anticollision as shown in FIGS. 12 and 13. When the output enable signal and the clock signal are applied, an address counter outputs memory read addresses one after another for each clock "L" pulse. Note that the data transmission rate in this case is 2fs / L (bit/sec). The memory sequentially outputs 2-bit information recorded at addresses designated by the address counter. A 1/4 frequency divider outputs a signal corresponding to 1/4 of fs. A shift register operates in accordance with the clock fs, and phase-shifts the output of the 1/4 frequency divider in units of 90°. When the output enable signal is applied, a data selector selects and outputs one of four phase outputs (0° to 270°) of the shift register in accordance with a 2-bit memory output.

[0030] However, it is possible to apply MPSK modulation by using a 1/M frequency divider, an M-stage shift register and an M-input data selector. In this case, it is possible to achieve the effect of increasing the amount of information that is transmitted per unit transmission power.

[0031] The output of the data selector changes the amplitude of current flowing through resistances to the PIN diodes D7 and D8 with a cycle of fs / 4, thereby modulating a connection impedance between the divided strip conductors. As shown in FIG. 14, the change of the impedance changes a mutual coupling impedance between an antenna of an interrogator and the antenna of the RFID tag, so that a reflection coefficient Γ of the antenna of the interrogator is changed with a cycle of fs / 4. FIG. 15 is an example of a signal measured with a spectrum analyzer. That is, from which it is possible to identify signal components ($f_0 + f_{LO}$, $f_0 + 3f_{LO}$, etc.), which are generated as a result of an incident wave of f_0 having been modulated by the change of Γ with a cycle of f_{LO}.

[0032] Incidentally, the microstrip antenna used for the RFID tag device of the present invention is explained with respect to its property. The microstrip antenna is configured simply by providing a ground plane close to a plate-like dipole antenna, and therefore might be considered as if it is an antenna that behaves as a dipole, but in fact, its behavioral principle is considerably different from that of the dipole antenna. Specifically, the dipole antenna is an electric current antenna, and the strip antenna is a magnetic current antenna. The reason why in the present invention, two PIN diodes for impedance modulation are provided at opposite ends of the

microstrip conductor in the width direction is that electric current flowing through the strip conductors is concentrated at the opposite ends in the width direction.

[0033] FIG. 16 is an example of analyzing the level of a response signal that can be received by an interrogator by using antenna length L as a parameter in the evaluation system of FIG. 14, with respect to the case where a conventional dipole antenna having no ground plate is used in an RFID tag and the case where the divided microstrip antenna of the present invention is used in an RFID tag. As can be seen from this figure, the method of the present invention is capable of receiving the response signal with a level greater by about 10 dB (10 times greater power) compared to the conventional method.

[0034] FIGS. 18 through 20 show changes in frequency at response receiver levels in the evaluation system of FIG. 14 with respect to design parameters w and h of the microstrip antenna (it is assumed that L is fixed). It can be appreciated from FIG. 18 that by reducing h (the thickness of an insulator), it is possible to make adaptation to lower frequencies with the same size (size reduction with the same frequency), but an available frequency bandwidth becomes narrow.

[0035] Also, it can be appreciated from FIG. 19 that by increasing w (the strip conductor width), it is possible to make adaptation to lower frequencies with the same size, but an available frequency bandwidth becomes narrow.

[0036] FIG. 20 is a result of analyzing influences of a series resistance in PIN diodes for impedance modulation that are exerted on the receiver level with respect to the cases of making adaptation to lower and higher frequencies with the same size. As can be seen from this figure, in the case of size reduction with the same frequency (reduction in h, increase in w), considerable influences are exerted by the series resistance of the PIN diodes, and therefore it is necessary to reduce the resistance in order to obtain a high response receiver level. In order to allow the PIN diodes to operate with low resistance, there is no choice but to apply a large current or increase junction capacitance (large area, short junction). The large current increases power consumption of the RFID tag device, and therefore is undesirable.

[0037] FIG. 21 is a result of analyzing a maximum response receiver level in the evaluation system of FIG. 14 by using the series resistance and junction

capacitance of the PIN diodes as parameters. As can be seen from this figure, the response receiver level does not change substantially when the junction capacitance of the PIN diodes is increased, and therefore it is possible to obtain a high response receiver level even by using relatively low-cost PIN diodes.

[0038] Also, instead of the PIN diodes, it is possible to use transistors such as MOSFET may also be used. In such a case, it is possible to further reduce the power consumption.

[0039] Also, when considering longitudinal connections of capacitors in a ladder boost rectifier circuit of a power receiving circuit as GND- and receiving-side rails, it is possible to consider diodes as rungs that join them. Capacitances of all the capacitors are normally equalized to maximize the booster efficiency, but in the present invention, the capacitor capacitance of the receiving-side rail is made smaller by one digit compared to that of the GND-side rail (specifically, GND-side rail: receiving-side rail = 1 : 0.05), and the first diode (between the GND and the receiving point) is eliminated, whereby it is possible to reduce input load capacity and receive a high-frequency and high-impedance input with a DC short.

(Example 2)

[0040] (A method for detecting the position of a moving object without an RFID tag)

The feature of the RFID tag of the present invention that is capable of relatively long range communication in spite of having no power supply is utilized.

[0041] Assuming that the positions of tags #1 through #4 and interrogators #1 and #2 are known as shown in FIG. 6, it is possible to estimate the position of a mobile object based on information concerning paths obstructed by the moving object.

[0042] In this case, a system may be configured such that $f_{m1} = f_{m2}$, $f_{s1} = f_{s2} = f_{s3} = f_{s4}$, the interrogators provide CW outputs in a time-division system, and the tags respond by an anticollision method.

[0043] Further, a system may be configured such that $f_{m1} \neq f_{m2}$, $f_{s1} = f_{s2} = f_{s3} = f_{s4}$, the interrogators successively provide CW outputs, and the tags respond by an anticollision method.

[0044] Furthermore, a system may be configured such that $f_{m1} \neq f_{m2}$, f_{s1}, f_{s2}, f_{s3} and f_{s4} are all different frequencies, and the interrogators successively

provide CW outputs.

(Example 3)

[0045] (A method for detecting the position of a moving object with RFID)

The feature of the RFID tag of the present invention that is capable of relatively long range communication in spite of having no power supply is utilized.

[0046] As shown in FIGS. 22 and 23, a plurality of receiving antennas are used at the master device, and CW signals are transmitted at two or more frequencies to detect differences in phase between response signals from RFID tags, making it possible to estimate three-dimensional locations of the RFID tags.

[0047] FIG. 7 illustrates the configuration of a master device. A Fourier transform section performs time-series Fourier integration on Re and Im data of antennas #1 through #4 to calculate a spectrum phase at a frequency Δ. In this case, it is assumed that phase differences due to each antenna cable and down converter and a time delay in operations of a selecting switch are calibrated for the compensation.

[0048] Note that FIG. 29 presents an example of an algorithm implemented in FORTRAN language for estimating three-dimensional locations of RFID tags in the configuration of FIG. 7, and FIG. 30 is an example of the program. Also, the analysis of RMS error in estimation of three-dimensional locations of the RFID tags in FIG. 23 is a result of computer simulation by the program of FIG. 29 using the number of receiving antennas and error in distance measurement as parameters.

(Example 4)

[0049] (A method for longer-range communication with RFID tags)

The RFID tag of the present invention, even by itself, can perform communication within a relatively long range of about 10 m. However, if it is used for a sign on an expressway and so on, the communication range of about 10 m is highly unlikely to be sufficient. Accordingly, RFID tags of the present invention are arranged in an array to add a phase difference to a response signal from each tag, so that the response signal can be returned with high sensitivity to interrogators in a wide area, thereby making it possible to perform communication within a range of about 100 m. An example thereof is shown in FIGS. 24 through 28.

[0050] The method described herein controls directionality by the

arrangement of the RFID tags and combinations of response signal phases at 0°/180° for each tag, however, it is also possible to more strictly control the directionality by assigning more fragmented phase differences as shown in FIG. 8.

[0051] Note that the combinations of phases at 0°/180° in FIG. 24 through 28 can be readily realized by using an EXOR as shown in FIG. 9.

BRIEF DESCRIPTION OF DRAWINGS

[0052]

FIG. 1 is a schematic diagram illustrating a conventional RFID tag device;

FIG. 2 is a schematic diagram illustrating an RFID tag device of the present invention;

FIG. 3 is a perspective view illustrating Example 1 of the present invention;

FIG. 4 is a top view illustrating a control circuit chip of the present invention;

FIG. 5 is a diagram illustrating an example of an impedance modulation element of the present invention;

FIG. 6 is a diagram illustrating Example 2 of the present invention;

FIG. 7 is a diagram illustrating Example 3 of the present invention;

FIG. 8 is a diagram illustrating Example 4 of the present invention;

FIG. 9 is a diagram illustrating Example 4 of the present invention;

FIG. 10 is a graph showing frequency response characteristics of a 10-stage Cockcroft-Walton circuit;

FIG. 11 is a graph showing frequency response characteristics of a 10-stage Cockcroft-Walton circuit;

FIG. 12 is a diagram showing a batch reading method for a plurality of RFIDs;

FIG. 13 is a graph showing a batch reading simulation for a plurality of RFIDs;

FIG. 14 is a diagram illustrating a planar antenna structure for RFID and a simulation model;

FIG. 15 is a graph showing an RFID response receiver frequency spectrum;

FIG. 16 is a comparison graph of receiver gain for modulated waves from RFID;

FIG. 17 a graph showing frequency response characteristics of a stub resonance boost rectifier circuit;

FIG. 18 is a graph for a comparison of RFID response receiver sensitivity frequency characteristics by changing a height between a microstrip line and GND;

FIG. 19 is a graph for a comparison of RFID response receiver sensitivity frequency characteristics by changing the width of a microstrip line;

FIG. 20 is a graph for a comparison of RFID response receiver sensitivity frequency characteristics with respect to resistance by changing a short resistance R of a PIN diode;

FIG. 21 is a graph showing receiver gain for modulated waves from microstrip RFID;

FIG. 22 is a diagram according to Example 3 of the present invention;

FIG. 23 is a diagram according to Example 3 of the present invention;

FIG. 24 is a diagram according to Example 4 of the present invention;

FIG. 25 is a diagram according to Example 4 of the present invention;

FIG. 26 is a diagram according to Example 4 of the present invention;

FIG. 27 is a diagram according to Example 4 of the present invention;

FIG. 28 is a diagram according to Example 4 of the present invention;

FIG. 29 is an exemplary FORTRAN program for estimating the three-dimensional location of an RFID tag;

FIG. 30 is an example of a FORTRAN program for estimating the three-dimensional location of an RFID tag.

EXPLANATIONS OF LETTERS OR NUMERALS

[0053]

D1, D2, D3, D4, D5, D6 Schottky-barrier diode

D7, D8 PIN diode

D9 Zener diode

ABSTRACT

PROBLEM TO BE SOLVED

The present invention aims to overcome the drawback with conventional RFID tag devices having a short communication range, and expand the communication range to several times or more that in the conventional scheme.

SOLUTION

The conventional scheme is based on equilibrium feeding/equilibrium modulation (a two-terminal circuit for antenna operation), whereas a method of the present invention is based on disequilibrium feeding/equilibrium modulation (a three-terminal circuit for antenna operation). The conventional scheme is based on simple rectification of received RF signals, whereas the present invention employs a circuit based on a combination of a stub resonance-based, impedance transformation boosting scheme and a ladder boosting scheme. The conventional scheme is based on ASK or BPSK modulation, whereas the present invention is based on passive modulation, but can employ a QPSK modulation circuit.

SELECTED FIGURE: FIG.2